UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,594	10/06/2003	Neil Johnson	ALT.P026	5941

27296 7590 05/19/2006

LAWRENCE M. CHO
P.O. BOX 2144
CHAMPAIGN, IL 61825

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/679,594	JOHNSON, NEIL	
	Examiner	Art Unit	
	Hashem Farrokh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,9-16 and 18-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,9-16,18,20-24,26-35,37* is/are rejected.

7)☒ Claim(s) *19,25 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The instant application having application No. 10/679,594 has a total of 37 claims pending in the application; claims 2, 7-8, and 17 have been canceled; claims 1, 3-6, 9-11, and 16 have been amended; claims 23-37 have been added.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 1, 3-5, and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5, 867,727 to Hattori in view of U.S. Patent Publication 2002/0152263 A1 to Goldrian et al. (hereinafter Goldrian) and U.S. Patent 5,557,750 to Moore et al. (hereinafter Moore).

1. In regard to claim 1, Hattori teaches:

"a data buffering unit," **(e.g., see column 9, lines 57 and 62; elements 38-1 to 38-8 and 46-1 to 46-8 in Fig. 12).** *The First-In-First-Out (FIFO) shown in Fig. 12 represents the buffering unit.*

"comprising:"

"a memory that includes a plurality of first-in-first-out (FIFO) memories **(e.g., see elements 38-1 to 38-8 and 46-1 to 46-8 in Fig. 12)** to stores data from a data

transmitting device;" **(e.g., see column 10, lines 51; elements 16 in Fig. 11).** *For example the Host Adapter 11 shown in Fig. 11 represents the transmitting device.*
"a memory write manager **(e.g., elements 22 and 58 in Fig. 15)** to determine which of the FIFO memories to access in response to a write address received from the data transmitting device **(e.g., elements 16 in Fig. 11)** and to write the data from the data transmitting device in the FIFO memories..." **(e.g., see column 11, lines 20-49; Fig. 15).** *For example the figure processor 22 and decoder 58 represents the write manage recited in the claim. The address bits A7 to A5 is used for selecting FIFOs. However, Hattori does not expressly teach: "...* writing to FIFO memories in a round robin fashion; a memory read manager that prepares data stored in the memory for output prior to receiving a request for the data from a data reading device."

Goldrian teaches: "... writing to FIFO memories in a round robin fashion;" **(e.g., see paragraph 71 in page 4)** *for writing to FIFOs in a round-robin fashion.*

Moore teaches: "a memory read manager **(e.g., see element 128 in Fig. 1)** that prepares data stored in the memory for output prior to receiving a request for the data from a data reading device." **(e.g., see column 1, line 67; column 2, lines 1-5; element 135 in Fig. 1)** *for prefetching the FIFO data and storing it into a prefetch register for outputting to the host prior to the host request.*
Disclosures by Moore, Goldrian, and Hattori are analogous because all references teach methods of managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the FIFO system taught by Hattori to include writing to FIFOs in round-robin fashion taught by Goldrian and prefetching disclosed by Moore.

The motivation for using round-robin as taught by paragraph 58, page 3 of Goldrian is to keep the packet sequence in order. Furthermore, the motivation for prefetching data as taught by column 2, lines 4-7 of the Moore to allow data to be available when the host request it, eliminating host waiting for an internal data bus cycle. By thus eliminating host waiting state, overall system performance is significantly enhanced.

Therefore, it would have been obvious to combined teaching of Moore and Goldrian with Hattori to obtain the invention as specified in the claim.

2. *In regard to claim 3, Hattori teaches*:

"wherein the memory read manager comprises a memory enable unit that asserts a read enable line to each of the plurality of FIFO memories." **(e.g., see column 15, lines 22-25; elements 46 and 52 and in Fig. 22).** *For example the control processor 42 and decoder 52 represent the read manager recited in the claim.*

3. *In regard to claim 4, Hattori teaches*:

"wherein the memory read manager comprises a read address manager that determines which of the plurality of FIFO memories to access in response to a read address from the data reading unit." **(e.g., see column 11, lines 60-67 to column 12, lines 1-5; elements 42, 70, and 74 in Fig. 15).** *For example the control processor 42, decoding circuit 70, and comparing circuit 74 represent the read manager recited in the claim.*

4. In regard to claim 5, Hattori teaches:

"wherein the memory read manager comprises a read selector **(e.g., MULTIPLEXER 144 IN Fig. 27)**, coupled to data outputs of each of the FIFO memories **(e.g., see element 126 in Fig. 26)**, that selects an appropriate data output to receive data from in response to a read address from the data reading device." **(e.g., see column 17, lines 66-67 to column 18, lines 1-5; Figs. 26-27).** *For example the output unit 128 (Fig. 26) include a multiplexer or selector 144 (Fig. 27) for selecting a word to be outputted.*

5. In regard to claim 9, Hattori teaches:

"wherein the write address manager determines a write address in one of the FIFO memories to write data in response to write address received from data transmitting device." **(e.g., see column 11, lines 39-59).**

6. In regard to claim 10, Hattori teaches:

"wherein the memory write manager **(e.g., see elements 22, 58 and 76 in Fig. 17)** comprises a write selector that transmits a write enable signal and data from the data transmitting device to an appropriate FIFO memory in response to the work address manager." **(e.g., see column 12, lines 52-64; element 60 in Fig. 17).** *For example the upper bit portion of address used to generate the select or enable signal 60 for writing to the selected FIFO.*

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori in view of Goldrian and Moore as applied to claim 1 above, and further in view of U.S. Patent 6,304,936 B1 to Shelock.

7. In regard to claim 6, Moore further teaches:

"the read pointer managers **(e.g., see element 128 in Fig. 1)** transmit an appropriate read address to each of the FIFO memories to prepare data to be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device." **(e.g., see column 1, line 67; column 2, lines 1-5; element 135 in Fig. 1).**

However, non of Hattori, Goldrian or Moore expressly teach: "wherein the memory read manager comprises a plurality of read pointer managers, each corresponding to one of the FIFO memories,"

Sherlock teaches: "the read pointer managers transmit an appropriate read address to each of the FIFO memories to prepare data to be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device." "wherein the memory read manager comprises a plurality of read pointer managers **(e.g., see column 5, lines 55-56)**, each corresponding to one of the FIFO memories," **(e.g., see column 8, lines 38-40)** *for providing read pointers to a plurality of FIFO memories.*

Disclosures by Sherlock, Moore, Goldrian, and Hattori are analogous because all references teach methods of managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the FIFO system taught by Hattori to include read pointers taught by Sherlock, writing to FIFOs in round-robin fashion taught by Goldrian, and prefetching disclosed by Moore.

The motivation for using read pointers as taught by column 1, lines 66-67 to column 2, lines 1-2 of Sherlock is to improve bandwidth efficiency and to reduce the circuit size and cost. Furthermore, the motivation for using round-robin as taught by paragraph 58, page 3 of Goldrian is to keep the packet sequence in order. Furthermore, the motivation for prefetching data as taught by column 2, lines 4-7 of the Moore to allow data to be available when the host request it, eliminating host waiting for an internal data bus cycle. By thus eliminating host-waiting state, overall system performance is significantly enhanced.

Therefore, it would have been obvious to combined teaching of Sherlock with Moore, Goldrian, and Hattori to obtain the invention as specified in the claim.

Claims 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherlock in view of Moore and U.S. Patent No. 6,891,397 B1 to Brebner.

8. *In regard to claim 11, Sherlock teaches:*

"memory blocks that form comprises a plurality of first-in-first-out (F1FO) memories that store data from a data transmitting device;" **(e.g., see column 11, lines 48-54; elements 1308 and 100 in Fig. 13).** *The element 100 represents the memory blocks and element 1308 represents the transmitting device recited in the claim. However, Sherlock does not expressly teach:* "logic elements that form a memory read manager that prepares data stored in the FIFO memories for output prior to a generation of a read address from a data reading device; A programmable logic device (PLD),"

Moore teaches: "a memory read manager that prepares data stored in the FIFO memories for output prior to a generation of a read address from a data reading device." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 23-24; element 135 in Fig. 1; Fig. 2)** *for using a prefetch register for having output data ready when the next bus cycle (e.g., bus cycle includes address) begins.*

Brebner teaches: "A programmable logic device (PLD)," **(e.g., see column 2, lines 22-24; column 7, lines 44-46; elements 326-1 to 326-4)** *for using PLD to implement logic and memory functions including FIFO buffers.*

Disclosures by Sherlock, Moore, and Brebner are analogous because all references teach methods of implementing and managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to include the PLD system disclosed by Berbner and the prefetch/restore mechanism taught by Moore to implement the bus bridge taught by Sherlock.

The motivation for including PLD as taught by column 1, lines 36-37 of the Brebner is to implement a system-level integration for flexibility and efficiency. Furthermore, the motivation for including the prefetch/restore mechanism as taught by column 2, lines 4-7 of the Moore is to allow data to be available when the host next bus cycle begins, eliminating host waiting for an internal data bus cycle. By thus eliminating host-waiting state, overall system performance is significantly enhanced.

Therefore, it would have been obvious to include teachings of Brebner and Moore to Sherlock to obtain the invention as specified in the claim.

9. *In regard to claim 12, Sherlock teaches:*

"wherein the memory read manager comprises a memory enable unit that asserts a read enable line to each of the plurality of FIFO memories." **(e.g., see column 11, lines 57-65; elements 100 and 1325 in Fig. 13).**

10. In regard to claim 13, Sherlock teaches:

"wherein the memory read manager comprises a read address manager that determines which of the plurality of FIFO memories to access in response to a read address from the data reading unit." **(e.g., see column 8, lines 36-64; element 414 in Fig. 4).**

11. In regard to claim 14, Sherlock teaches:

"wherein the memory read manager comprises a read selector coupled to data outputs of each of the FIFO memories **(e.g., see element 414 in Fig. 4; element 706 in Fig. 7)**, that selects an appropriate data output to receive data from in response to a read address from the data reading device." **(e.g., see column 6, lines 44-59; Fig. 7).**

12. In regard to claim 15, Sherlock teaches:

"wherein the memory read manager comprises a plurality of read pointer managers **(e.g., see column 5, lines 55-56)**, each corresponding to one of the FIFO memories," **(e.g., see column 8, lines 38-40)**. *However, Sherlock does not expressly teach:*

"the read pointer managers transmit an appropriate read address to each of the FIFO memories to prepare data to be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device."

Moore teaches: "the read pointer managers **(e.g., see element 128 in Fig. 1)** transmit an appropriate read address to each of the FIFO memories to prepare data to

be prepared for output on the FIFO memories prior to receiving a request for the data from the data reading device." **(e.g., see column 1, line 67; column 2, lines 1-5; element 135 in Fig. 1).** *The motivation for combining the two references is based on the same rational given in claim 1.*

Claims 16, 18, 20-21, 23-24, 26-35, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori in view of Moore.

13. *In regard to claim 16, Hattori teaches:*

"A method for managing data," **(e.g., see claim 16))** comprising:"

"selecting a first FIFO memory from a plurality of first-in-first-out (FIFO) memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device," **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.17).** *For example the address bits A7 to A5 coincide with the bits set in the FIFO is selected and the oldest (e.g., first data-in) data or first data is read out. However, Hattori does not expressly teach:* "wherein the first data was prepared for output prior to a generation of the first read address from the data reading device; and preparing next data from a next storage element from the first FIFO memory for output.

Moore teaches: "wherein the first data was prepared for output prior to a generation of the first read address from the data reading device;" **(e.g, see column 7, lines 66-67 to column 8, lines 1-3; Fig. 2)** *For preparing the next data for prefetching within a clock cycle.*

"preparing next data from a next storage element from the first FIFO memory for output." **(e.g, see column 7, lines 66-67 to column 8, lines 1-3; Fig. 2)** *For preparing data to be available in prefetch register for output.*

Disclosures by Moore and Hattori are analogous because both references teach methods of managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the FIFO system taught by Hattori to include prefetching disclosed by Moore.

The motivation for using prefetching data as taught by column 2, lines 4-7 of the Moore is to allow data to be available within one clock cycle, eliminating host waiting for an internal data bus cycle. By thus eliminating host-waiting state, overall system performance is significantly enhanced.

Therefore, it would have been obvious to combined teaching of Moore with Hattori to obtain the invention as specified in the claim.

14. In regard to claims 18, 30 and 35 Moore teaches:

"wherein the first data is output within a clock cycle after the first read address from the data reading device is generated." **(e.g., see column 7, lines 23-24; and lines 66-67 to column 8, lines 1-4; Fig. 2).**

15. In regard to claims 20, 26, and 31 Hattori teaches:

"selecting a second FIFO memory from the plurality of FIFO memories to output second data stored in a first storage element in the second FIFO memory in response to a second read address from the data reading device;" **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.15).** *Hattori teaches that first FIFO 38-1 and second FIFO 38-*

2 can be selected for reading by providing address bits 31 to 5 to decoding circuit 70 (e.g., see Fig. 15). Address 7 to 5 to select 1 of the 8 FIFOs 38-1 to 38-2. The control processors provide addresses A31 to A5 to decoding circuits for reading data from any of the 8 FIFOs. However, Hattori does not expressly teach: "preparing next data from a next storage element from the second FIFO memory for output."

Moore teaches: "preparing next data from a next storage element from the second FIFO memory for output." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 66-67 to column 8, lines 1-3; element 135 in Fig. 1; Fig. 2).**

16. In regard to claims 21, 27, 32 and 37 Hattori teaches: selecting any of plurality of 8 FIFOs for data output but does not expressly teaches:

"... preparing of the next data from the next storage element ..." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 66-67 to column 8, lines 1-3; element 135 in Fig. 1; Fig. 2).**

17. In regard to claim 23, Hattori teaches:

"A method for managing data **(e.g., see claim 16)**, comprising:"

"selecting a first FIFO memory from a plurality of first-in-first-out (FIFO) memories to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device," **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.17).** *For example the address bits A7 to A5 coincide with the bits set in the FIFO is selected and the oldest (e.g., first data-in) data or first data is read out. However, Hattori does not expressly teach:* "wherein the first data is output within a

clock cycle after the first read address is generated; and preparing next data from a next storage element from the first FIFO memory for output."

Moore teaches: "wherein the first data is output within a clock cycle after the first read address is generated;" **(column 7, lines 23-24; and lines 66-67 to column 8, lines 1-4; Fig. 2).**

"and preparing next data from a next storage element from the first FIFO memory for output." **(e.g, see column 7, lines 66-67 to column 8, lines 1-3; Fig. 2)** *For preparing the next data for prefetching within a clock cycle. The motivation for combining Moore with Hattori is based on the same rational given in claim 16.*

18. In regard to claims 24, 29, and 34 Moore teaches:

"wherein the first data was prepared for output by the first FIFO memory prior to a generation of the read address from the data reading device." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 66-67 to column 8, lines 1-3; element 135 in Fig. 1; Fig. 2).** *For example data is prepared and stored in prefetch register prior to next Bus cycle (e.g., prior to generation or read address).*

19. In regard to claim 28, Hattori teaches:

"A method for managing data **(e.g., see claim 16)**, comprising:"

"selecting a first FIFO memory from a plurality of first-in-first-out (FIFO) memories **(e.g., elements 38-1 to 38-8 in Fig. 12)** to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device;" **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.17).** *However, Hattori does not expressly teach:* "and preparing next data from a next storage element from the first

FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device."

Moore teaches: "and preparing next data from a next storage element from the first FIFO memory for output by transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 66-67 to column 8, lines 1-3; element 135 in Fig. 1; Fig. 2).** *The motivation for combining Moore with Hattori is based on the same rational given in claim 16.*

20. In regard to claim 33, Hattori teaches:

"A method for managing data **(e.g., see claim 16)**, *comprising:"*

"selecting a first FIFO memory from a plurality of first-in-first-out (FIFO) memories **(e.g., elements 38-1 to 38-8 in Fig. 12)** *to output first data stored in a first storage element in the first FIFO memory in response to a first read address from a data reading device;"* **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.15).**

"selecting a second FIFO memory from the plurality of FIFO memories to output second data stored in a first storage element in the second FIFO memory in response to a second read address from the data reading device;" **(e.g., see column 11, lines 60-67 to column 12, lines; Fig.15).** *Hattori teaches that first FIFO 38-1 and second FIFO 38-2 can be selected for reading by providing address bits 31 to 5 to decoding circuit 70 (e.g., see Fig. 15). Address 7 to 5 to select 1 of the 8 FIFOs 38-1 to 38-2. The control processors provide addresses A31 to A5 to decoding circuits for reading data from any*

of the 8 FIFOs. However, Hattori does not expressly teach: "preparing next data from a next storage element from the second FIFO memory for output."

Moore teaches: "preparing next data from a next storage element from the second FIFO memory for output." **(e.g., see column 1, line 67; column 2, lines 1-5; column 7, lines 66-67 to column 8, lines 1-3; element 135 in Fig. 1; Fig. 2).** *For example preparing data to be ready in prefetch register. The motivation for combining Moore with Hattori is based on the same rational given in claim 23.*

Claim 22 rejected under 35 U.S.C. 103(a) as being unpatentable over Hattori in view of Moore as applied to claim16 above, and further in view of Goldrian.

21. In regard to claim 22, the combined teaching of Hattori and Moore includes all limitations recited in claim 16 but does not expressly teach: "writing data into the plurality of FIFO memories in a round robin fashion."

Goldrian teaches: "writing data into the plurality of FIFO memories in a round robin fashion." **(e.g., see paragraph 71 in page 4)** *for writing to FIFOs in a round-robin fashion.*

Disclosures by Moore, Goldrian, and Hattori are analogous because all references teach methods of managing FIFO memories.

At the time of invention it would have been obvious to a person of ordinary skill in art to modify the FIFO system taught by Hattori to include writing to FIFOs in round-robin fashion taught by Goldrian and prefetching disclosed by Moore.

The motivation for using round-robin as taught by paragraph 58, page 3 of Goldrian is to keep the packet sequence in order. Furthermore, the motivation for prefetching data as taught by column 2, lines 4-7 of the Moore to allow data to be available when the host request it, eliminating host waiting for an internal data bus cycle. By thus eliminating host-waiting state, overall system performance is significantly enhanced. Therefore, it would have been obvious to combined teaching of Moore and Goldrian with Hattori to obtain the invention as specified in the claim.

ALLOWABLE SUBJECT MATTER

Claims 19, 25, and 36 are objected to as being dependent upon rejected based claims, but would be allowable if rewritten in correct and independent form including all of the limitations of the base claim and any intervening claims.

6. The primary reason for allowance of claims 19, 25, and 36 in instant application is the combination with the inclusion of the following limitations: **wherein preparing the next data from the next storage element from the first FIFO memory to output comprises transmitting a read address of the next storage element to the first FIFO memory prior to a request for the next data from the data reading device**

: IMPORTANT NOTE :

I f the applicant should choose to rewrite the independent claims to include the limitations recited in either one of the claims, the applicant is encouraged to ***amend the title of the invention*** *such that it is descriptive of the invention as claimed as required*

be sec. ***606.01*** *of the* ***MPEP****. Furthermore, the* ***summary of invention*** *and the* ***abstract*** *should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of* ***sec. 1302.01*** *of the* ***MPEP****.*

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not compiled with. See ***37 C.F.R. § 1.111(b)*** *and* ***§ 707.07(a) of the M.P.E.P.***

Response to Applicant Remarks

It has been noted that Applicant has amended some of the claims and has added new claims to include the allowable subject matters indicated in the previous Office Action. However, in view of newly discovered reference(s) the indicated allowability of claims are withdrawn. The Examiner would apologize if this causes any inconveniences.

Conclusion

The prior art made of record and not relied upon are as follows:

1. U. S. Patent No. 5,210,749 to Firoozmand describes Configuration of SRAMS as logical FIFOS for transmit and receive of packet data.

2. U. S. Patent No. 5,412,646 to Cyr *et al. describes Asynchronous transfer mode switch architecture.*

3. U. S. Patent No. 5,977,791 to Rubin et al. describes Embedded memory block with FIFO mode for programmable logic device.

Any inquiry concerning this communication should be directed to Hashem Farrokh whose telephone number is (571) 272-4193. The examiner can normally be reached Monday-Friday from ***8:00 AM to 5:00 PM.***

If attempt to reach the above noted Examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Donald A Sparks, can be reached on (571) 272-4201. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBS) at 866-217-9197 (toll-free).

HF

2006-05-14

DONALD SPARKS
SUPERVISORY PATENT EXAMINER